Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1. (Currently amended) An output stage comprising:

a p-channel inverter device coupled to a first supply voltage;

a p-channel stacked device coupled between the p-channel inverter and a pad;

an n-channel stacked device coupled to the pad; and

an n-channel inverter device coupled between the n-channel stacked device and a second supply voltage,

wherein a gate of the p-channel stacked device receives a first bias voltage and a gate of the n-channel stacked device receives a second bias voltage, and the first bias voltage and the second bias voltage vary depending on a voltage difference between the first supply voltage and the second supply voltage, and when a difference between the first supply voltage and the second supply voltage exceeds a voltage threshold, the first bias voltage is greater than the second supply voltage and the second bias voltage is less than the first supply voltage.

Claim 2. (Original) The output stage of claim 1 further comprising:

a first voltage translator coupled to a gate of the p-channel inverter device, wherein the first voltage translator translates a signal in a first voltage range to a second voltage range, the second voltage range defined by the first supply voltage and the second supply voltage.

Claim 3. (Original) The output stage of claim 2 further comprising:

a second voltage translator coupled to a gate of the n-channel inverter device, wherein the second voltage translator translates a signal in the first voltage range to the second voltage range.

Claim 4. (Original) The output stage of claim 3 wherein the second supply voltage is ground.

Claim 5. (Original) The output stage of claim 1 wherein the output stage is tri-stated by setting the first bias voltage approximately equal to the first supply voltage and the second bias voltage approximately equal to the second supply voltage.

Claim 6. (Cancelled)

Claim 7. (Original) The output stage of claim 5 wherein when the voltage difference between the first supply voltage and the second supply voltage is approximately equal to the sum of the drain-to-source breakdown voltages for the p-channel and n-channel inverter devices, the first bias voltage and the second bias voltage are approximately equal and near the mid-point between the first supply voltage and the second supply voltage.

Claim 8. (Original) The output stage of claim 7 wherein the bulk of the p-channel stacked device is coupled to a body bias circuit, and

wherein the body bias circuit generates a voltage that tracks the higher voltage between the first supply voltage and a received voltage.

Claim 9. (Original) An integrated circuit comprising:

an input stage coupled to a pad;

an output stage coupled to the pad; and

a bias circuit coupled to the pad

wherein the output stage comprises a first p-channel device coupled to the pad, the first p-channel device comprising a bulk, a drain, a gate, and a source, and the bulk is connected to the bias circuit, and

wherein the gate of the first p-channel device receives a first bias voltage, and the first bias voltage is selected based on a supply voltage received by the output stage.

Claim 10. (Original) The integrated circuit of claim 9 wherein the output stage further comprises:

a second p-channel device coupled to receive the supply voltage and further coupled to the first p-channel device.

Claim 11. (Original) The integrated circuit of claim 10 wherein the output stage further comprises:

a first n-channel device coupled to the first p-channel device, the first n-channel device comprising a gate,

wherein the gate of the first n-channel device receives a second bias voltage, and the second bias voltage is selected based on a supply voltage received by the output stage.

Claim 12. (Original) The integrated circuit of claim 10 further comprising:

a first voltage translator coupled to a gate of the first p-channel device, wherein the first voltage translator translates a signal in a first voltage range to a second voltage range, the second voltage range defined by the first supply voltage and a second supply voltage, wherein the second supply voltage is ground.

Claims 13 and 14. (Cancelled)

Claim 15. (Currently amended) ~~The integrated circuit of claim 14~~ An integrated circuit comprising:

an input stage coupled to a pad;

an output stage coupled to the pad and receiving a first power supply; and

a bias circuit coupled between the pad and the output stage,

wherein the output stage comprises a first p-channel device coupled to the pad, the first p-channel device comprising a bulk, a drain, a gate, and a source, the bulk connected to the bias circuit,

wherein the bias circuit comprises a first device and a second device coupled in series between the pad and the bulk of the first p-channel device, and

wherein a gate of the second device is coupled to the first power supply and a gate of the first device is coupled to a bias voltage, the bias voltage set to protect the first device from voltages on the pad.

Claim 16. (Currently amended) The integrated circuit of claim ~~13~~ 15 wherein the first device and the second device are p-channel devices.

Claim 17. (Currently amended) The integrated circuit of claim ~~13~~ 15wherein the output stage further comprises:

a second p-channel device coupled to receive the first supply voltage and further coupled to the first p-channel device, wherein the bulk of the first p-channel device is coupled to the bulk of the second p-channel device.

Claim 18. (Original) The integrated circuit of claim 17 further comprising:

a first voltage translator coupled to a gate of the first p-channel device, wherein the first voltage translator translates a signal in a first voltage range to a second voltage range, the second voltage range defined by the first supply voltage and a second supply voltage, wherein the second supply voltage is ground.

Claim 19. (Currently amended) ~~The integrated circuit of claim 13~~ An integrated circuit comprising:

an input stage coupled to a pad;

an output stage coupled to the pad and receiving a first power supply; and

a bias circuit coupled between the pad and the output stage,

wherein the output stage comprises a first p-channel device coupled to the pad, the first p-channel device comprising a bulk, a drain, a gate, and a source, and the bulk is connected to the bias circuit, and

wherein the bias circuit comprises a first device and a second device coupled in series between the pad and the bulk of the first p-channel device, the first device biased to protect the second device from voltages on the pad, and

wherein the first p-channel device receives a bias voltage at its gate, and the bias voltage is determined by the first supply voltage.

Claim 20. (Original) The integrated circuit of claim 19, wherein the integrated circuit is a programmable logic device.

Claim 21. (New) The integrated circuit of claim 15 wherein the bias circuit provides a bias voltage to the bulk of the first p-channel device, and the bias voltage tracks the higher voltage between the first supply voltage and a voltage on the pad.

Claim 22. (New) An integrated circuit comprising an output buffer, the output buffer comprising:

a first pull-up device coupled to receive a first supply voltage;

a second pull-up device coupled between the first pull-up device and a pad, and having a gate coupled to receive a first bias voltage;

a first pull-down device coupled to receive a second supply voltage;

a second pull-down device coupled between the first pull-down device and the pad, and having a gate coupled to receive a second bias voltage;

wherein when a difference between the first supply voltage and the second supply voltage is less than a first voltage threshold, the first bias voltage is approximately equal to the second supply voltage and the second bias voltage is approximately the first supply voltage, and

when the difference between the first supply voltage and the second supply voltage is greater than the first voltage threshold, the first bias voltage and the second bias voltage are each less than the first supply voltage and greater than the second supply voltage.

Claim 23. (New) The integrated circuit of claim 22 wherein when the difference between the first supply voltage and the second supply voltage is greater than a second voltage threshold, the first bias voltage and the second bias voltage are approximately equal and midway between the first supply voltage and the second supply voltage.

Claim 24. (New) The integrated circuit of claim 23 wherein when the difference between the first supply voltage and the second supply voltage is less than the second voltage threshold and greater than the first voltage threshold, the first bias voltage is between the second supply voltage and a voltage midway between the first supply voltage and the second supply voltage, and the second bias voltage is between the first supply voltage and a voltage midway between the first supply voltage and the second supply voltage.